Customer No.: 31561
Docket No.: 13353-US-PA
Application No.: 10/709,823

AMENDMENTS

To the Claims:

1. (original) A real-time data transmission interface suitable for transmitting a nonreal-time data in real-time and transmitting a real-time data in nonreal-time, and the real-time data transmission interface comprising:

a nonreal-time data interface unit for receiving/transmitting the nonreal-time data;

an I/O unit coupled to the nonreal-time data interface unit and being used as a transmission interface for the nonreal-time data and the real-time data;

a memory unit coupled to the I/O unit for caching the nonreal-time data and the real-time data; and

a network interface control unit coupled to the memory unit for receiving/transmitting the real-time data.

2. (original) The real-time data transmission interface of claim 1, wherein the nonreal-time data interface unit comprises:

a bus interface unit working as an interface for inputting/outputting the nonreal-time data;

a data output latch coupled to the bus interface unit via an internal data bus, wherein the data output latch is a latch for latching a data transmitted by the nonreal-time data interface unit to other units;

a data input latch coupled to the bus interface unit via the internal data bus, wherein the data input latch is a latch for latching a data transmitted by the other unit and received by the nonreal-time data interface unit;

a control signal latch coupled to the bus interface unit via the internal data bus, wherein the data output latch is a latch for latching a control signal transmitted by the nonreal-time data interface unit to other units;

a buffer coupled to the bus interface unit via the internal data bus; and

a flag register coupled to the buffer for storing a flag state.

3. (original) The real-time data transmission interface of claim 2, wherein the buffer comprises a 3-state (tri-state) buffer, when the flag state in the flag register is being setting/reading, the 3-state buffer is in an "on" state, while when the flag state is not being setting/reading, and the 3-state buffer is in a high impedance state.

4. (original) The real-time data transmission interface of claim 2, wherein the nonreal-time data interface unit further comprises a clock generator for generating and providing a clock signal to other units, and a frequency of the clock signal is 10MHz.

5. (original) The real-time data transmission interface of claim 1, wherein the I/O unit comprises:

a control logic unit for controlling the I/O unit to perform a read/write operation according to an external control signal;

a checking circuit coupled to the control logic unit, wherein when a self test mode is activated, the control logic unit controls the checking circuit to check an accuracy of the data output from the I/O unit and to generate a checking result;

a data output latch coupled to the control logic unit, wherein when the nonreal-time data is transmitted via the I/O unit, the control logic unit controls the data output latch to latch the nonreal-time data, and determines whether to output the nonreal-time data; and

a data input latch coupled to the control logic unit, wherein when the real-time data is read via the I/O unit, the data input latch receives the real-time data.

6. (original) The real-time data transmission interface of claim 1, wherein the memory unit comprises:

a control logic unit for controlling the memory unit according to an external control signal;

a first address counter coupled to the control logic unit for providing a first address;

a first memory coupled to the first address counter for storing the nonreal-time data;

a first buffer latch unit coupled to the first memory via an internal data bus for working as an input/output interface of the first memory;

a second address counter coupled to the control logic unit for providing a second address;

a second memory coupled to the second address counter for storing the real-time data; and

a second buffer latch unit coupled to the second memory via the internal data bus for working as an input/output interface of the second memory.

7. (original) The real-time data transmission interface of claim 6, wherein the memory unit further comprises a flag register for storing a flag state.

8. (original) The real-time data transmission interface of claim 1, wherein the network interface control unit comprises a programmable interface controller and a TTL/differential level converting interface, wherein the TTL/differential level converting interface is used to convert a type of the real-time data from TTL to differential or in reverse, and to cache the

real-time data.

9. (original) The real-time data transmission interface of claim 8, wherein the programmable interface controller comprises:

a storage apparatus, wherein a microcode is stored in the storage apparatus for controlling an operation of the programmable interface controller;

a sequencer coupled to the storage apparatus for running a microcode instruction and for adjusting a running order according to an external condition;

a condition selector coupled to the sequencer for caching the external condition, which is used by the sequencer for its determining;

an event/interrupt handler coupled to the storage apparatus for handling either an interrupt signal or an event;

a processor coupled to the storage apparatus for running the microcode instruction; and

a parity generating/checking apparatus for either generating a parity bit according to the real-time data output from the programmable interface counter or checking the parity bit of the real-time data input into the programmable interface controller.

10-18. (cancelled)